# **High-Performance and low-voltage current sense-amplifier using GAA-CNTFET with different chirality and channel**



Singh Rohitkumar Shailendra<sup>1,2</sup>, Pragya Sharma<sup>3</sup>, Dr. M. Aarthy<sup>3</sup>, Dr. Hidenori Mimura<sup>2</sup>

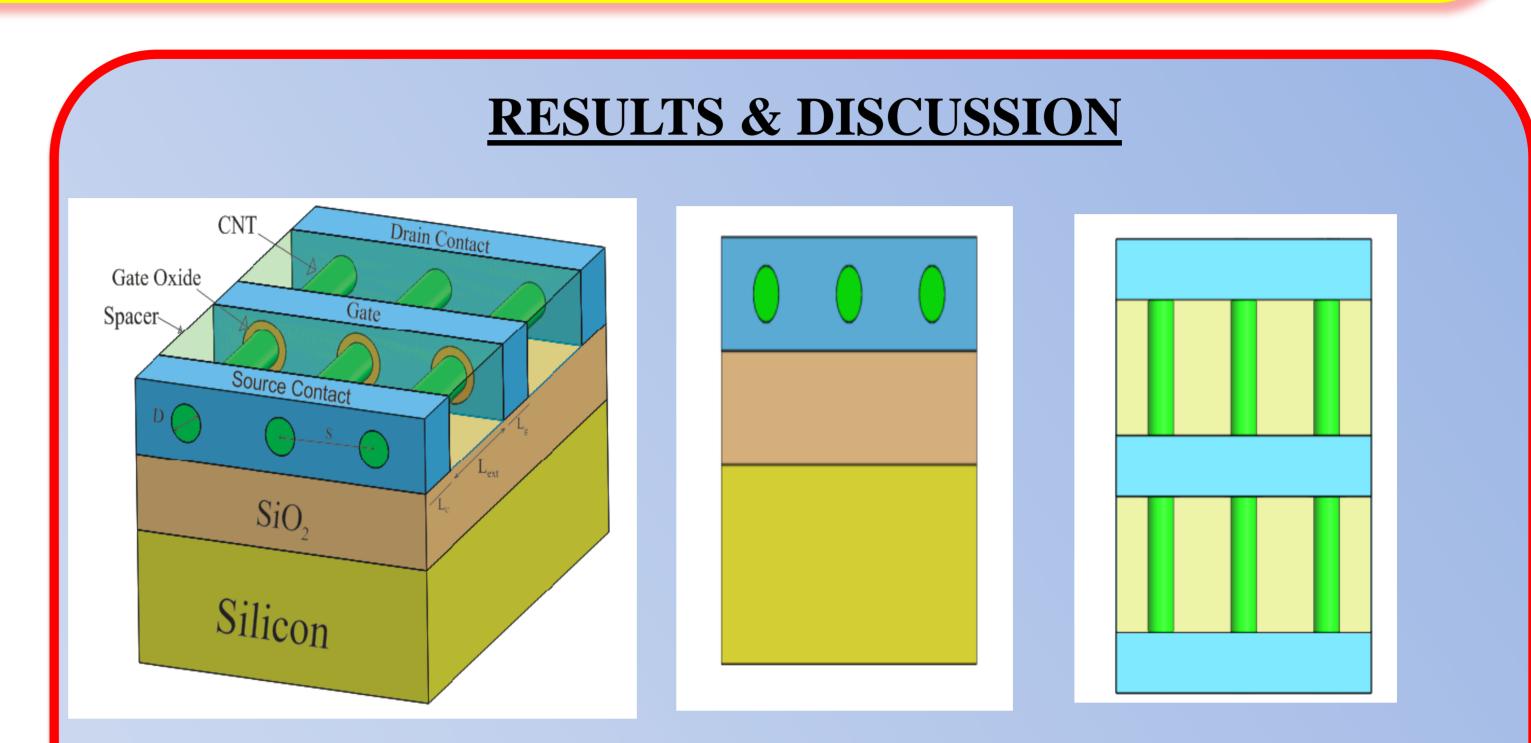


<sup>1</sup>Graduate School of Science and Technology, Shizuoka University, Hamamatsu, Japan <sup>2</sup>Research Institute of Electronics, Shizuoka University, Japan <sup>3</sup>School of Electronics Engineering, VIT, Vellore, India Email: rohitkumar.singh.19@shizuoka.ac.jp, pragyasharma1696@gmail.com



### **ABSTRACT**

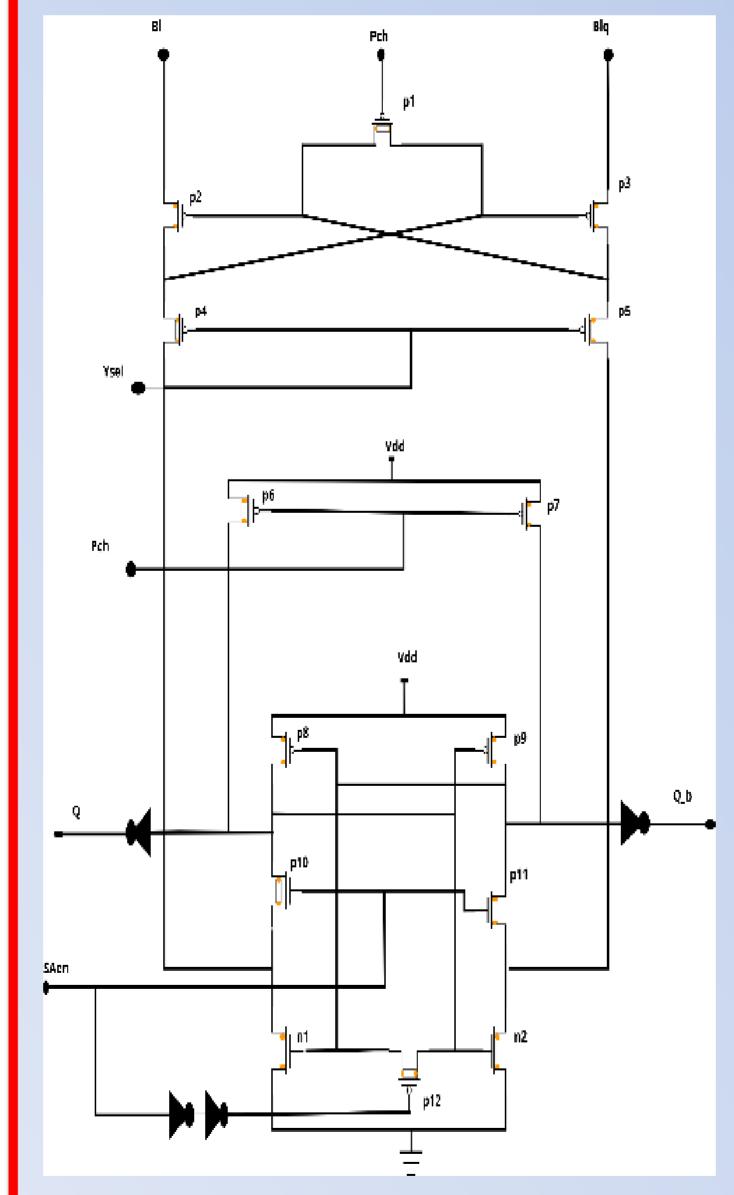
As scaling down of transistors have become the major concern these days, it has lead to the problems such as short channel effects, leakage current, high power consumption. To overcome these problems, CNTFETs are used which have proved itself as a promising device in the world of electronics. The property called as "Ballistic Transport" made it even popular. It led to the highly efficient conductivity of the current in the device. It is treated as the best replacement for MOSFETs. The parametric analysis has been carried out in this work for Current Sense amplifier for different chirality with different channels. Simulation results shows which combination of chirality, thickness oxide and dielectric constant is best suited for a specific application.

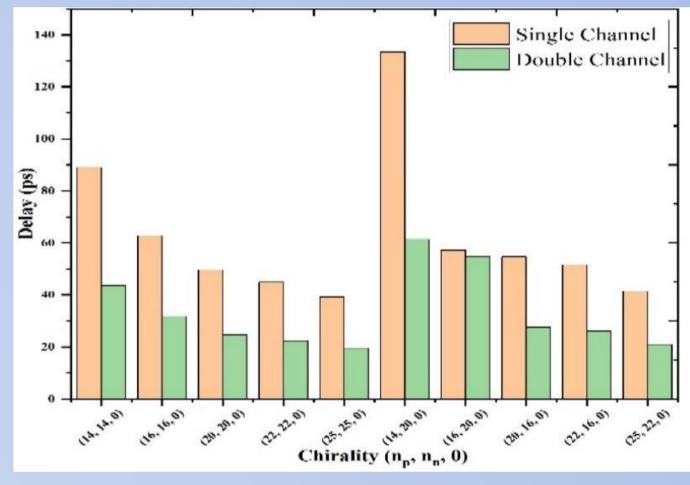


### **INTRODUCTION**

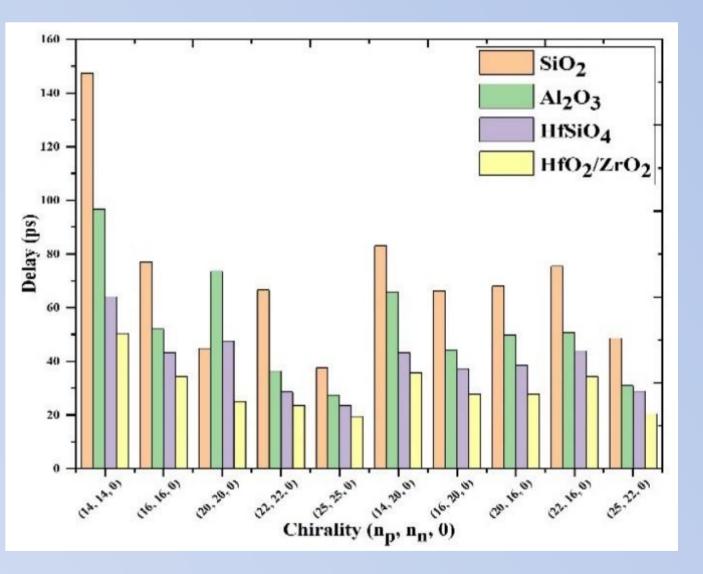
Moore's law states that the The transistor size in the integrated chip scales down by the factor of two for every two years. Since late twentieth century, scaling down of transistors has become the important factor for technology advancements, but it has also led to serious limitations in the performance of device such as short effects, channel passive power consumption, electron tunneling through short channels. This limitation are eliminated by using the field-effect transistor called CNTFET.

## GAA-Structure of CNTFET





Graph for Chirality vs. Delay of Single Channel and Double Channel CNTFETs



### **CONCLUSION**

Interpreting the simulation results, it is informed there is a significant trade-off between power consumption and delay in CNTFETs which is found based on the performance of amplifier built using CNTFETs. Based upon the application to be used the combination of chirality values, thickness oxide and dielectric oxide values should be choosen wisely to obtain optimal performance. • Circuit diagram of Current Sense Amplifier Graph for Chirality vs. Delay of Single Channel and Double Channel CNTFETs having the different value of K<sub>ox</sub>

#### **REFERENCES**

 1.S. lijima, "Helical Microtubules of Graphitic Carbon, Nature", Vol. 354, pp. 56-58, 1991
2. Geim A. K., Novoselov K. S.; (2007) *The rise of graphene* Nature Material, vol. 66, pp.183–191.
3. Zeitzoff, Peter M. "MOSFET scaling trends and challenges through the end of the roadmap." *Proceedings of the IEEE 2004 Custom Integrated Circuits Conference*, 2004.
4. Cho, Geunho, and Fabrizio Lombardi. "Design and process variation analysis of CNTFET-based ternary memory cells." *Integration* 54 (2016): 97-108.
5. Wong, H-S. Philip, et al. "Carbon nanotube device modeling and circuit simulation." Carbon Nanotube Electronics. Springer US, 2009. 133-162.